L Number	Hits	Search Text	DB	Time stamp
1	264	(micron adj technology) and capacitor and (storage adj node) and (cap or capping)	USPAT; US-PGPUB	2004/09/09 17:21
2	104	((micron adj technology) and capacitor and (storage adj node) and (cap or capping)) and @ad<19990902	USPAT; US-PGPUB	2004/09/09 17:03
3	6	(micron adj technology) and capacitor and (storage adj node) and (cap or capping)	EPO; JPO; DERWENT; IBM_TDB	2004/09/09 17:21

L Number	Hits	Search Text	DB	Time stamp
1	2852	438/253,255,396,398,666.ccls. and capacitor and @ad<20020222	USPAT; US-PGPUB	2004/09/14 16:26
3	1441	257/306-309.ccls. and capacitor and @ad<20020222	USPAT; US-PGPUB	2004/09/14 16:27
4	544	(257/306-309.ccls. and capacitor and @ad<20020222) and (storage near3 node)	USPAT; US-PGPUB	2004/09/14 16:27
5	422	((257/306-309.ccls. and capacitor and @ad<20020222) and (storage near3 node)) not ((438/253,255,396,398,666.ccls. and capacitor and @ad<20020222) and (storage near3 node))	USPAT; US-PGPUB	2004/09/14 16:27
2	1043	(438/253,255,396,398,666.ccls. and capacitor and @ad<20020222) and (storage near3 node)	USPAT; US-PGPUB	2004/09/14 16:28

DERWENT-ACC-NO: 1998-398062

DERWENT-WEEK: 200048

TITLE: Forming an isolated contact to a DRAM bit line - has pairs of **capacitor** pillars surrounding bit nodes, with a silicon oxide **cap** formed on each pillar, by a series of mask and etch steps

INVENTOR: FIGURA, T A; PAN, P

PATENT-ASSIGNEE: **MICRON TECHNOLOGY** INC[MICRN]

PRIORITY-DATA: 1995US-0523072 (September 1, 1995)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5776815 A	July 7, 1998	N/A	021	H01L 021/20

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
US 5776815A	N/A	1995US-0523072	September 1, 1995

INT-CL (IPC): H01L021/20

RELATED-ACC-NO: 2000-531675

ABSTRACTED-PUB-NO: US 5776815A

BASIC-ABSTRACT:

A bit line contact is formed by forming a pair of pillar-type capacitors (24), one on each side of a bit node (28). They have **storage node** layers, a cell dielectric layer and a common cell conductive layer. An

oxide barrier is added
over the common conductor. An oxide barrier layer is formed, and remove from
the pillar tops. An oxide **cap** (48) is then grown on each pillar. A mask is
formed on the caps and the intervening barrier oxide is removed. A conformal
dielectric (70) of silicon nitride is formed, followed by a filling dielectric
(72) containing borophosphosilicate glass over the exposed conductor. The
dielectric layers are masked and etched to form a bit node contact region (76).

ADVANTAGE - Simple isolation of the bit contact is provided and the presence of
the oxide caps allows a greater contact target area to be opened between the
capacitors than if the caps were not present.

CHOSEN-DRAWING: Dwg.14/14

TITLE-TERMS: FORMING ISOLATE CONTACT DRAM BIT LINE PAIR **CAPACITOR** PILLAR
SURROUND BIT NODE SILICON OXIDE **CAP** FORMING PILLAR SERIES MASK ETCH
STEP

DERWENT-CLASS: L03 U11 U12 U13 U14

CPI-CODES: L03-G04A; L04-C06; L04-C11; L04-C12A; L04-C12B; L04-C12D; L04-C14A;

EPI-CODES: U11-C05G1B; U11-C05G2C; U12-C02A1; U13-C04B1A; U14-A03B4;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C1998-120482
Non-CPI Secondary Accession Numbers: N1998-309699

US-PAT-NO: 6214727

DOCUMENT-IDENTIFIER: US 6214727 B1

TITLE: Conductive electrical contacts, capacitors, DRAMs, and integrated circuitry, and methods of forming conductive electrical contacts, capacitors, DRAMs, and integrated circuitry

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Brief Summary Text - BSTX (15):
In one aspect, the invention includes a method of forming a capacitor storage node in a shape of a vertically elongated stem underlying a **cap, the cap** having a first cross-sectional dimension of equal to or greater than a minimum capable photolithographic feature dimension of a fabrication process, the stem having a second cross-sectional dimension of less than the first cross-sectional dimension.

Detailed Description Text - DETX (18):
As shown, the combination of first opening 92 and fourth opening 110 preferably forms an opening having a shape of a vertically elongated stem 113 underlying a **cap** 115. Similarly, the combination of openings 93 and 111, and the combination of openings 94 and 112 comprise shapes of vertically elongated stems 113 underlying caps 115. It is noted that the respective caps and stems will both preferably comprise cross-sectional dimensions of less than the minimum capable photolithographic feature dimension obtainable during fabrication. Preferably, stems 110, 111 and 112 will have

cross-sectional dimensions of about the minimum cross-sectional dimensions of narrowed constrictions 106, 107 and 108 in FIG. 9. However, the cross-sectional dimensions of stems 110, 111 and 112 may be slightly larger than the dimensions of constrictions 106, 107 and 108, as the constriction openings may be widened somewhat by removal of layers 102 and 104 from the sides of the constriction openings as the layers 102 and 104 are etched from the bases of openings 92, 93 and 94.

Detailed Description Text - DETX (22):

Referring to FIG. 12, an upper surface of wafer fragment 10a is removed. Preferably, such removal planarizes the remaining upper surface of wafer fragment 10a. Such planarization may be accomplished, for example, by chemical-mechanical polishing or other techniques. Preferably, the planarization removes layer 36a (shown in FIG. 11) to expose a surface 126 of insulative layer 34a. Surface 126 may be identical to the original upper surface 35a of insulative layer 34a or may be beneath the original surface 35a of insulative layer 34a. The planarization to below layer 36a electrically isolates conductive pedestals 116, 117 and 118 from one another. As shown, the preferred isolated pedestals 116, 117 and 118 have the shape of a **cap** 115 over a stem 113, as did the openings discussed above with reference to FIG. 10.